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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/389,321	09/03/1999	TOSHIRO HIRAMOTO	026350-028	5290

21839 7590 09/25/2002

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ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 09/25/2002

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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Paper No. 17

Application Number: 09/389,321
Filing Date: September 03, 1999
Appellant(s): HIRAMOTO ET AL.

Ellen Marcie Emas
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 18 June 2002.

(1) Real Party in Interest

A statement identifying the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

A statement identifying the related appeals and interferences which will directly affect or be directly affected by or have a bearing on the decision in the pending appeal is contained in the brief.

(3) Status of Claims

The statement of the status of the claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Invention

The summary of invention contained in the brief is correct.

(6) Issues

The appellant's statement of the issues in the brief is correct.

(7) Grouping of Claims

Appellant's brief includes a statement that claims 2 and 8, claims 3 and 9, claims 4 and 10, claims 5 and 11, and claims 1, 6, 7, and 12 do not stand or fall together and provides reasons as set forth in 37 CFR 1.192(c)(7) and (c)(8).

(8) Claims Appealed

The copy of the appealed claims contained in the Appendix to the brief is correct.

(9) Prior Art of Record

5,698,885 WARASHINA et al. 12-1997

(10) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

A. Definitions of certain claim terms.

Applicant's specification makes the following definitions:

1. Of the terms applicant uses, it is found that MOS and DTMOS are terms used fairly often by those skilled in the art, where it is understood that a MOS has a gate, oxide or similar gate insulator, source, drain, and channel region, while a DTMOS in addition has an electrical connection between the gate and the channel region. Application at page 2 lines 12-24.
2. EIB, electrically induced body, and EIB-MOS, are terms for which no reference can be found in general use. Outside of the current application, the examiner has only found these terms in an English abstract of JP 2000260991 A, which is the laid-open copy of applicant's priority document. According to applicant these terms may also be found in a paper presented by the applicant and a co-author to the 1998 International Electron Devices Meeting of the IEEE. This is not taken to be sufficient evidence that these terms are in general use and these terms are defined herein strictly with reference to applicant's specification as filed. EIB, electrically induced body, and EIB-MOS all appear to refer to an SOI MOS adapted for biasing the voltage of the substrate relative to the body, i.e. channel region. Application at page 9, lines 7-11. For brevity, the examiner has adopted this terminology and the examiner has coined, in addition, the term EIB-FET, to refer to any SOI FET, either MOS, Schottky gated, or junction, which is adapted for biasing the voltage of the substrate of the SOI relative to the body of the FET.
3. VTMOS is an EIB-MOS where the substrate voltage bias may be switched from a first voltage to a second, lower bias. Application at page 2, lines 7-11.
4. Accumulation mode means a FET with its channel having the same conductivity as its drain and source.

B. Claims 1, 2, and 4-6, and 7,8, and 10-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over BURR et al. (6,100,567).

With regard to all claims, particularly independent claims 1 and 7 Burr discloses a pair of FETs (field effect transistors) comprising an SOI (502, 504) which includes a substrate (552, 554) composed of a semi-conducting material, a single crystal semi-conducting layer (512, 514, 516 or 520, 522,524), an insulating oxide substrate (508) where the semi-conducting layer (512, 514,

516), is made of a source (512, 520), drain (514, 522), and a surrounded (characterized as a "body" region in claim 7) region (516, 524) that is surrounded by the source (512, 520) and the drain (514, 522). Burr further discloses a connection (544, 546) that adapts the substrate (540, 542) to be applied with a voltage of a first polarity (and in fact is applied with a voltage of a first polarity, thus meeting claim 7), and a depletion region, i.e. a depletion layer (328). Note figs. 3, 5, and column 1, line 27 of Burr. Note that independent claim 7 repeats the recitals of independent claim 1, with the substitution of the words "threshold voltage controlled by changing a body potential of the MOS transistor" for the words "" in the preamble, substitution of the words "body region" for the words "surrounded region" in lines 7 and 8, and substitution of the words "is applied with a voltage" for "is adapted to be applied with a voltage" in line 10. Burr does not teach an MOS because although Burr teaches a conductive polysilicon layer which functions as a gate, Burr does not explicitly show an insulating film for insulating that gate from the surrounded region (for example, the words "gate insulating film" or "gate oxide" do not appear in Burr's disclosure). Rather Burr teaches that the conductive polysilicon layer functions as a gate, with no particular means specified for achieving the gate. Thus the most that can be said for the teachings of Burr is that it discloses an EIB-FET and not an EIB MOS FET. Further, Burr does not explicitly teach that charges of a second polarity are induced the composition surface in the depletion layer that is in contact with the insulating layer.

However, it would have been clear that an insulator could be placed between the transistor body and Burr's gate to form an FET of the MOS type. In context, the "composition surface" is the depletion layer surface in contact with the insulating layer. One skilled in the art would understand that applying a voltage to the conductive substrate would cause all surfaces, including the one opposing the composition surface, to have that voltage. One skilled in the art would further understand that when placed in opposition to a surface having voltage of first polarity, the surface of a conductive body such as the depletion layer would carry charges of second polarity. Therefore, it would be obvious to one of ordinary skill the art to build an FET of the MOS type according to the teachings of Burr, in order to obtain the advantages of an FET with variable threshold voltage taught by Burr. It would be obvious that that FET would include a composition surface in the depletion layer in contact with the insulating layer in which charges of a second polarity are induced.

With specific regard to independent claims 6 and 12, Burr teaches the step of applying a voltage of a first polarity to the substrate of an EIB-FET, and that this step controls the threshold voltage. See Burr, column 6 table 1. For this reason, it would have been obvious to one of ordinary skill in the art to perform the same step with a EIB-MOS which includes a semiconducting substrate, a semiconducting single crystal layer, an insulating oxide interposed between, source, drain and surround regions, depletion layer and composition surface, in order to tune the performance of the FET, as taught by Burr.

With further regard to claims 2 and 8, Burr teaches a DT-FET where the undepleted channel region is electrically connected to the gate. With an oxide layer between gate and channel, this FET would be a DTMOS transistor. See fig. 2, esp. part 230. It would have been obvious to one of ordinary skill in the art to combine Burr's DT-FET with Burr's EIB-FET and place an insulator between the transistor body and Burr's gate to form a DT-MOS, that is, a DT-FET of the MOS type, in order to combine the voltage threshold reduction realized by the DT-FET, as

taught by Burr, with the variable threshold voltage advantages of the EIB-FET, as taught by Burr.
With further regard to claims 4 and 10, applicant defines VTMOS as a transistor in which the threshold voltage is controlled by "(the) whole of a chip" in which the VTMOS transistor is provided, or alternatively, as a transistor where a first voltage is applied to the substrate in the "active mode," and a second, smaller, voltage is applied in the "standby mode." Application, page 2, lines 8-11. The term VTMOS, as a claim term, is herein read as defined in the specification. Using applicant's second definition, a VTMOS is a transistor where a first voltage is applied to the substrate and at some other time (alternatively) a second, smaller, voltage is applied to the substrate instead of the first voltage. A VTMOS, so defined, would have been obvious to one of ordinary skill in the art under the same analysis used for the EIB-MOS.
With further regard to claims 5 and 11, it is noted that the pair of transistors disclosed by Burr form a CMOS (complementary MOS) circuit.

C. Claims 3 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Burr in view of WARASHINA, et al. (5,698,885)

Burr discloses an EIB-FET with all the limitations of claim 3 except the MOS gate structure, composition surface, induced charges of second polarity, and accumulation mode, i.e. channel having same conductivity as introduced carriers. Warashina et al. discloses a MOS FET in accumulation mode. The MOS FET is known to reduce power by limiting gate current. Warashina et al. describe accumulation mode as reducing power by reducing threshold voltage. Burr describes the EIB-FET as reducing power by reducing threshold voltage. Therefore, it would have been obvious to one of ordinary skill in the art to combine the MOS-FET of Warashina et al. with the EIB-FET of Burr, in order to reduce power consumption.

(11) Response to Argument

It is argued, at page 7 of the remarks, that "the design [disclosed by Burr] is constrained by the diode leakage between the p and n conductive regions" However, it is noted that the features upon which applicant relies (i.e., the lack of diode leakage between p and n regions) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).
It is argued, at page 8 of the remarks, that "nothing in Burr shows, teaches or suggests a surrounded or body region including a depletion layer ... [r]ather Burr merely discloses a depletion region 328." (the emphasis is original) The examiner submits that this argument is purely a matter of semantics. Burr's depletion region 328 has all the characteristics of a layer, as the term layer is commonly understood.
It is argued, at page 8 of the remarks, that "the Examiner has admitted that EIB, electrically induced body [it should be noted that the words 'electrically induced body' do not appear in the claims] and EIB-MOS are terms which cannot be found outside of Applicants' work. However, the Examiner [misinterprets] what this means" The Examiner's understanding of the meaning of these acronyms comes from page 9 lines 7-11 of the application which state:

> When the negative voltage V_{sub} is adapted to be applied to the substrate 20, electrons are introduced into the substrate 20. That is, a p type neutral region which is not present in the conventional fully depleted SOI MOS transistor is provided in the body electrically by the voltage V_{sub}. The MOS transistor having such a structure is referred to an (sic) Electrically Induced Body ((EIB-MOS) transistor.

The Examiner takes the position that two statements included in the above quote, namely "electrons are introduced into the substrate 20" and "a p type neutral region which is not present in the conventional fully depleted SOI MOS transistor is provided in the body electrically," are statements of applicants' particular theories concerning the physics of the device and do not define structure. For this reason the Examiner concluded that Applicant defines EIB and EIB-MOS as an SOI MOS transistor having a structure which is adapted for the application of a negative voltage V_{sub} to the substrate thereof.

It is argued, at page 8 of the remarks, that "[I]n the amendment filed 8/19/2002, Applicants provided the Examiner with four references to provide definitions of a EIB." However, the Examiner believes that in determining the meaning of claim terms, the law requires him to ignore these references, since they are not U.S. patents. The incorporation of essential material in the specification by reference to a foreign application or patent, or to a publication is improper. See *In re Hawkins*, 486 F.2d 569, 179 USPQ 157 (CCPA 1973); *In re Hawkins*, 486 F.2d 579, 179 USPQ 163 (CCPA 1973); and *In re Hawkins*, 486 F.2d 577, 179 USPQ 167 (CCPA 1973).

It is argued, at page 9 of the remarks, that "that the present invention differs from Burr according to the features listed in the table." However, these features are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

It is argued, at page 12 of the remarks, that "Nothing in Warashina et al. shows, teaches, or suggests ... a EIB-DTMOS transistor comprising an accumulation mode EIB-DTMOS transistor having a channel which is doped with impurities so that the channel has the same conductivity type as that of carriers introduced into the channel." In response to applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986). Warashina et al. discloses a p-channel SOI/MOSFET of an accumulation mode (AM) type. Note column 7 line 15 of Warashina et al. Examining Burr in view of Warashina et al suggests the combination of an EIB-DTMOS in accumulation mode.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

tld
September 19, 2002

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